REMARKS

The Office Action dated July 8, 2005 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-32 are currently pending in the application and are respectfully resubmitted for consideration.

Claims 1-9, 14-22 and 27-32 were rejected under 35 U.S.C. §102(a) as being anticipated by *LEVEL ONE* (Level One™ IXP1200 Network Processor). The above rejection is respectfully traversed according to the remarks that follow.

Claim 1, from which claims 2-13 depend, recites a network switch for network communications. The network switch includes a first data port interface supporting at least one data port transmitting and receiving data and a second data port interface supporting at least one data port transmitting and receiving data. The switch also has a CPU interface configured to communicate with a CPU, a common memory communicating with the first data port interface and the second data port interface, and a memory management unit for communicating data from the first data port interface and the second data port interface and the common memory. The switch also has at least two sets of communication channels, with each of the communication channels communicating data and messaging information between the first data port interface, the second data port interface, and the memory management unit. One set of communication channels of at least two sets of communication channels provides communication from the first and second data port interfaces to the memory management unit and another set of communication channels of at least two sets of communication channels provides

communication from the memory management unit to the first and second data port interfaces. Additionally, the first data port interface, the second data port interface, the CPU interface, the common memory, the memory management unit and the at least two sets of communication channels are embodied on a single substrate.

Claim 14, from which claims 15-26 depend, recites a network switch for network communications. The network switch includes first data means supporting at least one data port transmitting and receiving data and second data means supporting at least one data port transmitting and receiving data. The switch also includes interface means configured to communicate with a CPU, means for storing data communicating with the first data means and the second data means and means for managing memory and communicating data from the first data means and the second data means and the means for storing data. The switch also includes at least two sets of communication channel means, with each of the communication channel means communicating data and messaging information between the first data means, the second data means, and the means for managing memory. One set of communication channel means of at least two sets of communication channel means provides communication from the first and second data means to the means for managing memory and another set of communication channel means of at least two sets of communication channel means provides communication from the means for managing memory to the first and second data means. Additionally, the first data means, the second data means, the interface means, the means

for storing data, the means for managing memory and the at least two sets of communication channel means are embodied on a single substrate.

Claim 27, from which claims 28-32 depend, recites a method of handling data packets in a network switch. The method includes the steps of receiving at a data port an incoming data packet, resolving a destination address of the incoming data packet, discarding, forwarding, or modifying the packet based upon the resolving step and placing at least a portion of the data packet on a first communication channel. When the packet is to be forwarded, a section of another data packet is received at the data port on a second communication channel from a common memory and the another data packet is forwarded from the data port, where the first and second channels are separate from each other and the steps are performed in a single network switch on a single substrate.

As discussed in the present specification, the present invention provides a network device that is compact and provides necessary processing power in a single chip embodied on a single substrate. It is respectfully submitted that the cited prior art fails to disclose or suggest all of the elements of any of the presently pending claims. Therefore, the prior art fails to provide the critical and unobvious advantages discussed above.

LEVEL ONE is directed to a network processor that is used to switch data on a network. The Office Action points to Figure 1 of *LEVEL ONE* as teachings multiple data port interfaces, a CPU interface, common memory, a MMU and "at least two set [sic] of communication channels for communicating data and messaging information." The Response to Arguments section of the last Office Action, it was acknowledged that the

"10/100/1Gb Ethernet MAC" and the "ATM, T1/E1, Other MAC" are equivalent to the data port interfaces recited in the independent claims. However, Applicants respectfully assert that *LEVEL ONE* fails to teach or suggest all of the elements of claims 1, 14 and 27.

Claims 1, 14 and 27 recite, in part, that "the first data port interface, the second data port interface, the CPU interface, the common memory, the memory management unit and the at least two sets of communication channels are embodied on a single substrate." Looking to Figure 1 of *LEVEL ONE* and its associated description, the "10/100/1Gb Ethernet MAC" and the "ATM, T1/E1, Other MAC" are discussed, but those interfaces are not on the IXP 1200 Network Processor. Both are clearly disclosed as being external to the IXP 1200 Network Processor. Thus, for at least this reason, Applicants respectfully assert that the rejection of claims 1, 14 and 27 is improper and should be withdrawn.

The network processor does have an "IX Bus Interface Unit" and a "PCI Bus Unit," but if those units were taken as equivalent to the first and second data port interfaces, there would be no disclosure of the CPU interface by *LEVEL ONE*. In other words, the independent claims 1, 14 and 27 all recite three interfaces embodied on a single substrate and *LEVEL ONE* only discloses two interfaces that the Office Action has identified as communication interfaces. Thus, in the Response to Arguments section, it is asserted that "the PCI Bus Unit is for interfacing to the Host CPU and the PCI MAC Devices, and the IX Bus Interface Unit is for interfacing to 10/100/1Gb Ethernet devices,

and other devices," that is only two interfaces. Since claims 1, 14 and 27 recite that "the first data port interface, the second data port interface, the CPU interface, the common memory, the memory management unit and the at least two sets of communication channels are embodied on a single substrate," *LEVEL ONE* does not teach all of the elements of those claims and cannot be validly applied as an anticipatory reference.

Additionally, in the Response to Arguments section, it is also asserted that the device in *LEVEL ONE* supports sixteen 10/100 ports and that "a single wire connecting an external device to the switch can also be considered an interface." While it is acknowledged that an Examiner during the examination of claims in prosecution of a patent application must give terms in pending claims their broadest reasonable interpretation, that interpretation must be consistent with the specification. See M.P.E.P 2111. The term "interface" in the instant specification has a particular meaning, such as, for example, in paragraph [0025] where it is used in the context of a Gigabit Port Interface Controller (GPIC) and a CPU Management Interface Controller (CMIC). As such, redefining an "interface," in the context of the instant application, to mean "a single wire" is not consistent with the instant specification. In addition, it should also be pointed out that such a redefinition of "interface" would also be inconsistent with that term's use in *LEVEL ONE* as well.

In addition, no memory controlled by the memory management unit is disclosed as being resident in the IXP 1200 Network Processor; rather the SDRAM, SRAM, Boot ROM and the peripherals are disclosed as being external to the IXP 1200 Network

Processor. Claims 1, 14 and 27 all recite that the memory management unit controls the memory such that any other memory in the Network Processor cannot be used to teach or suggest that element. Therefore, even though the Response to Arguments section alleges that SDRAM Memory Unit, SRAM Memory Unit and data cache are internal memories, they cannot be used to teach or suggest the internal memory embodied on a single substrate, as recited in the claims. In addition, given the disclosure of *LEVEL ONE*, it is not clear that the SDRAM and SRAM Memory Units have any memory for storing packet data and may merely be used to control access to those memories. Thus, Applicants respectfully assert that all of the elements in claims 1, 14 and 27 are not taught by *LEVEL ONE* and the rejection of those claims should be withdrawn.

In addition, it is also not clear from the *LEVEL ONE* disclosure that the IXP 1200 Network Processor is "embodied on a single substrate," as provided in claims 1, 14 and 27. The Office might alleges that it would be obvious to have all of the elements be embodied on a single substrate, but such reasoning would not be permitted in the rejection of claims 1, 14 and 27, which is made under 35 U.S.C. §102(b). Thus, for at least this reason, Applicants respectfully assert that the rejection of claims 1, 14 and 27 is improper and should be withdrawn.

Additionally, Applicants also respectfully assert that subject matters of claims 1, 14 and 27 are also not rendered obvious over *LEVEL ONE*. Given the disclosed structure of the network processor in *LEVEL ONE*, and the benefits of the components discussed in Section 2 of *LEVEL ONE*, one of ordinary skill in the art would not be motivated to

embody all off the external units onto a single substrate. If the proposed modification would render the modified prior art reference to be unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Thus, Applicants respectfully assert that the subject matter of claims 1-9, 14-22 and 27-32 is neither taught nor suggested by *LEVEL ONE*.

Claims 10, 11, 23, 24 and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over *LEVEL ONE* in view of *Hegde* (U.S. Patent No. 6,570,875). Claims 12 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over *LEVEL ONE* in view of *Bray et al.* (U.S. Patent No. 6,483,849). The Office Action acknowledges that *LEVEL ONE* fails to teach or suggest all of the elements of those claims. Because of this, the Office Action also cites *Hegde* and *Bray et al.* in the alleged rejections of those claims. *Hegde* is cited for its alleged teachings of the use of a VLAN table and *Bray et al.* is cited for its alleged teachings of auto-negotiation. However, even if the latter references were accepted for what they are alleged to teach, which is not admitted, they would not cure the deficiencies of *LEVEL ONE* noted above. As such, Applicants respectfully traverse the rejection of claims 10-13 and 23-26 for at least their dependence on claims 1 and 14.

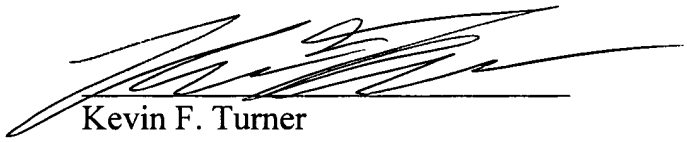
In view of the above, Applicants respectfully submit that claims 1-32 each recite subject matter which is neither disclosed nor suggested by *LEVEL ONE*, *Hegde* and *Bray*

et al. It is therefore respectfully requested that all of claims 1-32 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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